over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

64. (Amended) An integrated circuit comprising:

a semiconductor substrate;

a transistor formed on the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact [within a contact] opening in the insulating layer, the contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

68. (Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device formed on the semiconductor substrate, the electronic device having an active region;

a borophosphous silicate glass (BPSG) layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of a contact [within a contact] opening in the borophosphous silicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

72. (Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of [within] a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

77. (Amended) An integrated circuit comprising:

a semiconductor substrate;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy covering the walls and bottom of [within] a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

81. (Amended) An integrated circuit comprising:

a semiconductor substrate;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain

region;

a borophosphous silicate glass (BPSG) layer over the source/drain region;

an alloy layer of a titanium alloy covering the walls and bottom of [within] a high aspect ratio contact opening in the borophosphous silicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

83. (Amended) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy covering the walls and bottom of [within] a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the alloy layer is produced using a method including:

forming a seed layer supported by a substrate by combining a first precursor with a first reducing agent; and

forming the titanium layer supported by the substrate by combining a titanium-containing precursor with the seed layer.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on July 18, 2002, and the references cited therewith.

Claims 44, 60, 64, 68, 72, 77, 81, and 83 are amended, no claims are canceled, and no claims are added; as a result, claims 44-45 and 60-83 are now pending in this application.